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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,907	07/17/2003	Huajun Wen	AUS920030431US1	2143

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IBM CORPORATION (CS)
C/O CARR LLP
670 FOUNDERS SQUARE
900 JACKSON STREET
DALLAS, TX 75202

EXAMINER	
DIMYAN, MAGID Y	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/621,907	WEN, HUAJUN	
	Examiner	Art Unit	
	Magid Y. Dimyan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action pertains to Application No. 10/621,907 filed July 17, 2005. Claims 1 – 17 remain pending in this Application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 – 5 and 12 – 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Jones (U.S. Patent No. 6,813,753).

4. Regarding claim 1, Jones teaches a method for designing a circuit comprising a plurality of conductors (see col. 1, lines 13 – 29), the method comprising: (a) selecting a first and second operating points corresponding to a first and second circuit operations (see col. 2, lines 6 – 14); (b) determining a performance difference between circuit operations at the first and second operating points, and using the performance

difference to compute a factor (see col. 2, lines 27 – 42; col. 3, lines 49 – 57); and (c) applying the factor to resistance values of the conductors to produce modified resistance values (see col. 1, lines 33 – 37; col. 2, lines 43 – 51), and performing timing analysis of the circuit using modified values (see col. 1, lines 26 – 29; col. 20, lines 1 – 19). Thus, Jones clearly cites all the claimed limitations.

5. As per claims 2 and 3, see again col. 1, lines 13 – 28; col. 20, lines 1 – 19, which show how simulations and model testing (i.e., timing analysis) can be used to verify correct circuit operation/performance requirements in the presence of circuit constraints, as claimed.

6. Pursuant to claim 4, see col. 1, lines 5 – 10 and lines 25 - 29, which cite an Integrated Circuit. An SoC is a commonly used type of an Integrated Circuit, and is well known in the art of IC design.

7. As for claim 5, see col. 1, lines 20 – 28, which recite the claimed element of the interconnectivity routing between cells.

8. Referring to claims 12 and 13, see Fig. 13, block 135; col. 15, line 65 – col. 16, line 65 which disclose how the scaling factor is determined by computing a ratio based on circuit performance at two operating points and using that factor to determine performance difference.

9. As per claim 14, see col. 1, lines 13 – 29, which teach the IC being designed using the method of claim 1, as claimed.

10. Regarding claims 15, 16 and 17, Jones discloses a computer apparatus and system for designing an IC (Fig. 17; col. 19, line 47 – col. 20, line 19) comprising a plurality of conductors (col. 1, lines 13 – 29) that includes: (a) means for applying a factor to resistance values of the conductor thereby producing modified values (col. 1, lines 30 – 45; col. 2, lines 27 – 51; col. 20, lines 12 – 19); and (b) means for performing timing analysis of the circuit using modified resistance values (col. 1, lines 24 – 28; col. 20, lines 1 – 19). Thus, Jones teaches all the claimed limitations.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 6 – 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones in view of Publication No. 2004/0025136 to Carelli, JR. (hereinafter, "Carelli").

13. The teachings of Jones pertaining to a method and system for designing a circuit comprising a plurality of conductors by generating and using a scaling factor based on different operating points of a circuit application are recited above, and described in more detail in his disclosure. However, Jones does not disclose the use of a 3 – dimensional environment space having a process dimension, a power supply dimension and a temperature dimension, nor does he disclose selecting the first and second operating points within the environment window or near the edge of the window as claimed. On the other hand, Carelli recites a method for designing a custom ASIC library that uses interpolation techniques (i.e. applying a factor) to generate a technology cell library from an existing cell library (see Figs. 2 and 5; page 2, paragraphs 0015 – 0023). Furthermore, Carelli teaches the 3 – dimensional environment space that includes voltage, temperature and processing dimension in his disclosure (paragraphs 0012;0013; 0024), and also shows how the operating points are selected within the environment window (Fig. 2; paragraphs 0012 – 0014; paragraphs 0030 – 0033). Using a 3 – dimensional environment window that includes processing, voltage and temperature information is commonly used in IC design in order to achieve a robust IC design while maximizing fabrication and manufacturing yield. It would therefore be obvious to a person of ordinary skill in the art to combine the teachings of Jones and Carelli to obtain the same claimed inventions.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y. Dimyan whose telephone number is (571) 272-1889. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Magid Y Dimyan
Examiner
Art Unit 2825

myd
03 August 2005

MYD

VUTHE SIEK
PRIMARY EXAMINER